FORM PTO-1390 (Modified) (REV 10-95) U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE

TRANSMITTAL LETTER TO THE UNITED STATES DESIGNATED/ELECTED OFFICE (DO/EO/US) CONCERNING A FILING UNDER 35 U.S.C. 371

ATTORNEY'S DOCKET NUMBER: **194310US2PCT**

U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR): 09/582630

INTERNATIONAL APPLICATION NO.	INTERNATIONAL FILING DATE	PRIORITY DATE CLAIMED
PCT/FR99/00155	**27 January 1999**	**28 January 1998**

TITLE OF INVENTION

PROCESS FOR FABRICATING A STRUCTURE OF SEMICONDUCTOR-ON-INSULATOR TYPE, IN PARTICULAR SICOI

APPLICANT(S) FOR DO/EO/US

Lea DI CIOCCIO

Applicant herewith submits to the United States Designated/Elected Office (DO/EO/US) the following items and other information:

1. ☒ This is a **FIRST** submission of items concerning a filing under 35 U.S.C. 371.
2. ☐ This is a **SECOND** or **SUBSEQUENT** submission of items concerning a filing under 35 U.S.C. 371.
3. ☒ This is an express request to begin national examination procedures (35 U.S.C. 371(f)) at any time rather than delay examination until the expiration of the applicable time limit set in 35 U.S.C. 371(b) and PCT Articles 22 and 39(1).
4. ☒ A proper Demand for International Preliminary Examination was made by the 19th month from the earliest claimed priority date.
5. ☒ A copy of the International Application as filed (35 U.S.C. 371 (c) (2))
   a. ☐ is transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☒ has been transmitted by the International Bureau.
   c. ☐ is not required, as the application was filed in the United States Receiving Office (RO/US).
6. ☒ A translation of the International Application into English (35 U.S.C. 371(c)(2)).
7. ☒ A copy of the International Search Report (PCT/ISA/210).
8. ☒ Amendments to the claims of the International Application under PCT Article 19 (35 U.S.C. 371 (c)(3))
   a. ☐ are transmitted herewith (required only if not transmitted by the International Bureau).
   b. ☐ have been transmitted by the International Bureau.
   c. ☐ have not been made; however, the time limit for making such amendments has NOT expired.
   d. ☒ have not been made and will not be made.
9. ☐ A translation of the amendments to the claims under PCT Article 19 (35 U.S.C. 371(c)(3)).
10. ☒ An oath or declaration of the inventor(s) (35 U.S.C. 371 (c)(4)).
11. ☐ A copy of the International Preliminary Examination Report (PCT/IPEA/409).
12. ☐ A translation of the annexes to the International Preliminary Examination Report under PCT Article 36 (35 U.S.C. 371 (c)(5)).

Items 13 to 18 below concern document(s) or information included:

13. ☐ An Information Disclosure Statement under 37 CFR 1.97 and 1.98.
14. ☐ An assignment document for recording. A separate cover sheet in compliance with 37 CFR 3.28 and 3.31 is included.
15. ☒ A **FIRST** preliminary amendment.
    A **SECOND** or **SUBSEQUENT** preliminary amendment.
16. ☐ A substitute specification.
17. ☐ A change of power of attorney and/or address letter.
18. ☐ Certificate of Mailing by Express Mail
19. ☒ Other items or information:

Request for Consideration of Documents Cited in International Search Report
Notice of Priority
PCT/IB/304
PCT/IB/308
Drawings (2 sheets)

534 Rec'd PCT/PTC 26 JUL 2000

U.S. APPLICATION NO. (IF KNOWN, SEE 37 CFR) 09/582630	INTERNATIONAL APPLICATION NO. PCT/FR99/00155	ATTORNEY'S DOCKET NUMBER 194310US2PCT

20. The following fees are submitted:.

BASIC NATIONAL FEE (37 CFR 1.492 (a) (1) - (5)) :

		CALCULATIONS PTO USE ONLY
☒	Search Report has been prepared by the EPO or JPO	**$840.00**
☐	International preliminary examination fee paid to USPTO (37 CFR 1.482)	**$670.00**
☐	No international preliminary examination fee paid to USPTO (37 CFR 1.482) but international search fee paid to USPTO (37 CFR 1.445(a)(2))	**$760.00**
☐	Neither international preliminary examination fee (37 CFR 1.482) nor international search fee (37 CFR 1.445(a)(2) paid to USPTO	**$970.00**
☐	International preliminary examination fee paid to USPTO (37 CFR 1.482) and all claims satisfied provisions of PCT Article 33(2)-(4)	**$96.00**

ENTER APPROPRIATE BASIC FEE AMOUNT =	**$840.00**	
Surcharge of **$130.00** for furnishing the oath or declaration later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (e)).	**$0.00**	

CLAIMS	NUMBER FILED	NUMBER EXTRA	RATE		
Total claims	13 - 20 =	0	x $18.00	**$0.00**	
Independent claims	1 - 3 =	0	x $78.00	**$0.00**	
Multiple Dependent Claims **(check if applicable)**.			☐	**$0.00**	
TOTAL OF ABOVE CALCULATIONS =				**$840.00**	
Reduction of 1/2 for filing by small entity, if applicable. Verified Small Entity Statement must also be filed (Note 37 CFR 1.9, 1.27, 1.28) **(check if applicable).**			☐	**$0.00**	
SUBTOTAL =				**$840.00**	
Processing fee of **$130.00** for furnishing the English translation later than ☐ 20 ☐ 30 months from the earliest claimed priority date (37 CFR 1.492 (f)). +				**$0.00**	
TOTAL NATIONAL FEE =				**$840.00**	
Fee for recording the enclosed assignment (37 CFR 1.21(h)). The assignment must be accompanied by an appropriate cover sheet (37 CFR 3.28, 3.31) **(check if applicable).**			☐	**$0.00**	
TOTAL FEES ENCLOSED =				**$840.00**	
				Amount to be: refunded	$
				charged	$

☒ A check in the amount of **$840.00** to cover the above fees is enclosed.

☐ Please charge my Deposit Account No. in the amount of to cover the above fees.
A duplicate copy of this sheet is enclosed.

☒ The Commissioner is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. **15-0030** A duplicate copy of this sheet is enclosed.

NOTE: Where an appropriate time limit under 37 CFR 1.494 or 1.495 has not been met, a petition to revive (37 CFR 1.137(a) or (b)) must be filed and granted to restore the application to pending status.

SEND ALL CORRESPONDENCE TO:

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SIGNATURE

Marvin J. Spivak
NAME

24,913
REGISTRATION NUMBER

July 26, 2000
DATE

194310US2 PCT

IN THE UNITED STATES PATENT & TRADEMARK OFFICE

IN RE APPLICATION OF:

LÉA DI CIOCCIO : ATTN: APPLICATION DIVISION

SERIAL NO: NEW U.S. PCT APPLICATION
(Based on PCT/FR99/00155)

FILED: HEREWITH : EXAMINER:

FOR: PROCESS FOR FABRICATING A STRUCTURE OF SEMICONDUCTOR-ON-INSULATOR TYPE, IN PARTICULAR SICOI

PRELIMINARY AMENDMENT

ASSISTANT COMMISSIONER FOR PATENTS
WASHINGTON, D.C. 20231

SIR:

Prior to a first examination on the merits, please amend the above-identified application as follows:

IN THE SPECIFICATION

Page 1, before line 1, insert:

--TITLE OF THE INVENTION--;

actual line 3, delete in its entirety and substitute therefor:

--BACKGROUND OF THE INVENTION

Field of the Invention--;

prenumbered line 25, delete in its entirety and substitute therefor:

--Discussion of the Background--.

Page 4, prenumbered line 29, delete in its entirety and substitute therefor:

line 25, delete "(12)".

Claim 4, line 2, delete "(10)";

line 3, delete "(12)".

Claim 5, line 2, delete "(12)";

last line, delete "(10)".

Claim 6, line 2, delete "(14)";

line 3, delete "(12)".

Claim 7, line 2, delete "(20)";

line 3, delete "(24)";

line 4, delete "(10)";

line 5, delete "(12)";

last line, delete "(24)".

Claim 8, line 1, delete "or 3".

Claim 9, line 2, delete "(12)";

last line, delete "(12)".

Claim 10, line 2, delete "(12)" and "(30)".

Claim 11, line 2, delete "(12)";

last line, delete "(20)".

Please add new Claim 13 as follows:

--13. Process according to claim 3, in which the insulator is an oxide.--

--SUMMARY OF THE INVENTION--.

Page 9, line 1, delete in its entirety and substitute therefor:

--BRIEF DESCRIPTION OF THE DRAWINGS--;

prenumbered lines 24-25, delete in their entirety and substitute therefor:

--DESCRIPTION OF THE PREFERRED EMBODIMENTS--.

IN THE CLAIMS

Please amend the claims as follows:

Claim 1, line 2, delete "(20)";

line 3, delete "(12)";

line 5, delete "(12)";

line 6, delete "(10)";

line 9, delete "(16)";

line 11, delete "(18)" and "(10)";

line 12, delete "(12)";

line 13, delete "(10)";

line 14, delete "(12)";

line 15, delete "(20)";

line 16, delete "(12)";

line 17, delete "(20)";

line 19, delete "(16)";

line 20, delete "(18)";

line 22, delete "(12)" and "(20)";

line 24, delete "(18)";

IN THE ABSTRACT OF THE DISCLOSURE

Please delete the abstract sheet in its entirety and insert therefor:

--ABSTRACT OF THE DISCLOSURE

A process for fabricating a structure including a carrier substrate and a layer of semiconductor material on one surface of the carrier substrate. The process a) forms a layer of semiconductor material on one surface of a first substrate, b) forms a cleavage zone in the first substrate, which delimits a superficial layer, c) transfers the first substrate, with the layer of semiconductor material, onto the carrier substrate, d) provides energy to cause cleavage of the first substrate along the cleavage zone, and e) removes said superficial layer to uncover the layer of semiconductor material.--

REMARKS

Favorable consideration of this application, as presently amended, is respectfully requested.

The present preliminary amendment is submitted to place the above-identified application in more proper format under United States practice. By the present preliminary amendment the specification has been amended to include suggested headings. The claims have been amended to no longer recite any reference numerals or multiple dependencies. The subject matter of the cancelled multiple dependencies is also now submitted in new dependent Claim 13. A new abstract believed to be in more proper format under United States practice is also submitted herein.

The present application is believed to be in condition for a full and through examination on the merits. An early and favorable consideration of the present application is hereby respectfully requested.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
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PROCESS FOR FABRICATING A STRUCTURE OF SEMICONDUCTOR-ON-INSULATOR TYPE, IN PARTICULAR SiCOI

Technical field

This invention relates to a particular process for fabricating a structure comprising a carrier substrate and a layer of semiconductor material on one surface of the carrier substrate.

More particularly, it concerns the forming of a semiconductor-on-insulator structure such as, for example, a structure of silicon carbide-oxide-semiconductor type.

The invention finds applications in the areas of microelectronics and optoelectronics for the fabrication of substrates such as substrates comprising a GaN layer. This material is a semiconductor with a wide forbidden band and allows the fabrication of electro-optic devices such as electroluminescent diodes or lasers which operate in the ultraviolet and blue spectrum.

The invention also finds applications in the manufacture of microsystems able to operate in hostile environments, such as high temperature environments or corrosive atmospheres. In this case, with the process of the invention it is possible, for example, to provide thin membranes of silicon carbide able to withstand the stresses of the hostile environment.

Prior art

As indicated previously, gallium nitride (GaN) is a material of particular interest on account of its wide forbidden band for the fabrication of electro-optical devices. For such applications, however, it

proves to be impossible to obtain monocrystalline GaN blocks of sufficient size.

Therefore, at the present time, substrates are made which comprise one layer of GaN that subjected to heteroepitaxial growth on a sapphire or silicon carbide (SiC) substrate.

The use of sapphire as epitaxial substrate leads to obtaining GaN layers having a high density of crystalline defects. By using silicon carbide (SiC) as epitaxial substrate, it is possible to obtain better crystalline quality - since there is better mesh parameter agreement between GaN and SiC.

The very high cost of monocrystalline SiC substrates is, however, a handicap in its use for epitaxial growth.

On account of the high cost of monocrystalline SiC substrates, it is possible to have recourse to more economical substrates which only comprise a thin superficial layer of SiC on the surface of a basic substrate in silicon.

However, silicon, silicon carbide and the gallium nitride that is subsequently formed have fairly different thermal dilatation coefficients. Considerable stresses and a high defect density therefore occur during the formation of the gallium nitride on this type of substrate.

This problem may be at least partly solved by providing an oxide layer between the silicon and the silicon carbide. This layer brings a reduction in the stresses due to differential dilatation and leads to obtaining a so-called "compliant" substrate.

In known manner, it is for example possible to fabricate structures of silicon carbide-on-insulator

type (SiCOI), by forming a layer of SiC through epitaxy on a substrate of silicon-on-insulator type (SOI).

In such cases, however, a thin film of silicon remains from the superficial silicon layer of the SOI, between the SiC and the oxide. This silicon film causes some loss of the "compliant" properties obtained with the oxide layer of the SOI structure. Also, during SiC epitaxy, cavities are formed in the oxide layer and defects occur in the SiC layer.

It is also possible to conduct carburization of the superficial silicon layer of a substrate of silicon-on-insulator (SOI) type, to convert it entirely into SiC and thereby obtain a SiC/Oxide interface with no intermediate silicon.

This solution, however, proves to be difficult to implement insofar as the superficial silicon layer of SOI structures generally has a thickness of a few hundred nanometres. The carburization of silicon only enables a SiC layer to be obtained over a thickness that is in the order of a few dozen nanometres.

Document (1), whose reference is specified at the end of this disclosure, puts forward another process for obtaining a "compliant" substrate comprising a silicon carbide layer on an oxide layer.

According to this document, an oxide layer is formed on the surface of a solid SiC substrate and ions are implanted in the substrate to create a weakened zone therein. This weakened zone delimits in the substrate a superficial layer of SiC in contact with the oxide layer.

The SiC substrate, provided with the oxide layer, is then transferred to a target substrate in silicon by contacting the oxide layer with the target substrate.

Finally heat treatment is applied to cause cleavage of the SiC substrate along the weakened zone and release the superficial SiC layer. This layer remains integral with the target substrate via the insulator layer.

The cleavage of a substrate along a weakened zone using heat treatment is also described in document (2) whose reference is also specified at the end of this disclosure.

The structure finally obtained therefore has, in the following order, a silicon substrate, an oxide layer then a silicon carbide layer.

With the process described above, it is possible to obtain carriers with a SiC layer which are less costly than substrates in monocrystalline SiC. The process does however have a certain number of limitations.

It appears that a relatively high heat schedule (treatment time-treatment temperature) is required for cleavage of the silicon carbide. This heat schedule is for example 1 hour at 850°C. By way of comparison, cleavage of silicon may be brought about with a schedule of only 30 seconds at 500°C.

Also, the cleaved silicon carbide proves to have surface roughness. The SiC surface therefore has to be treated by polishing before other semiconductor materials, such as GaN, can be formed on this surface.

Description of the disclosure

The purpose of the invention is to put forward a process for fabricating a structure comprising a carrier substrate and a layer of semiconductor material on one surface of this substrate, such as a structure

of silicon-on-insulator type, and in particular silicon carbide on insulator, which does not encounter the difficulties or limitations set forth above.

One purpose in particular is to put forward an economical process for fabricating a structure of silicon carbide-oxide-silicon type which does not require a high heat schedule during the cleavage operation.

Another purpose is to propose such a process with which it is possible to obtain a SiC layer having excellent surface condition.

A further purpose is also to put forward a process for fabricating carriers for a GaN layer.

Yet a further purpose is to enable a large-size structure to be obtained (in particular with SiC or GaN layers).

To achieve these purposes, the invention sets out more specifically to propose a process for fabricating a structure comprising a carrier substrate and a layer of semiconductor material on one surface of the carrier substrate, the process comprising the following successive steps:

a) forming a layer of semiconductor material on one surface of a first substrate,

b) implanting ions in the first substrate, underneath said surface, in the vicinity of the layer of semiconductor material, to form a zone, called a cleavage zone, which delimits a superficial layer in the first substrate, in contact with the layer of semiconductor material,

c) transferring the first substrate, with the layer of semiconductor material, onto the carrier substrate,

the layer of semiconductor material being made integral with the carrier substrate,

d) providing energy to cause cleavage of the first substrate along the cleavage zone, the superficial layer of the first substrate remaining integral with the layer of semiconductor material and with the carrier substrate during cleavage,

e) removing said superficial layer to uncover the layer of semiconductor material.

According to one advantageous embodiment, the supply of energy for step d) is chosen from among a supply of thermal energy, mechanical energy, or a combination of these energies.

By supply of thermal energy is meant the application of heat treatment.

This heat treatment may be applied using a heat schedule that is determined in relation to the different heat schedules used throughout the process. In particular, this heat treatment may take into account overheating induced by heat treatments of off-thermodynamic equilibrium type such as those which may result from the ion implantation step, and by heat treatments using substrate heating or cooling such as for implantation for example, or possible reinforcement of bonding forces when bonding to a support.

This heat treatment may also give consideration to the use of other supplies of energy such as the application of mechanical forces.

Hence, at step d), the heat treatment may be zero, the supply of energy in this case possibly only being in mechanical form.

According to one advantageous embodiment of the invention, removal step e) is conducted using a removal

process chosen from among wet or dry chemical etching, polishing, oxidation followed by etching, or a combination of these modes.

According to one particular aspect of the invention, between steps a) and b), or between steps b) and c), the layer of semiconductor material may be subjected to treatments such as in particular treatments to fabricate active and/or passive components. If components are fabricated before step b), these treatments are then taken into account to determine the conditions of ion implantation.

According to one particular embodiment of the invention, the first substrate may be a silicon substrate, and the layer of semiconductor material may be a layer of silicon carbide.

It is seen that, in this case, the cleavage made at step d) of the process does not occur in a layer of silicon carbide, but in the silicon of the first substrate. Cleavage may then be caused with a lower heat schedule which, moreover, leaves intact the layer of silicon carbide.

In addition, the process of the invention is adapted to the fabrication of structures with a layer of semiconductor material, SiC in particular, which have a very large surface area.

During step c) of the process, the layer of semiconductor material may be made integral with the substrate by means of heat treatment.

The same heat treatment may be extended and made use of to cause the cleavage in step d) of the process.

In order to obtain a final structure with good "compliant" properties, for which the differences in thermal dilatation coefficients only have little

effect, an oxide layer may be provided between the layer of semiconductor material and the carrier substrate. This is of particular advantage if the layer of semiconductor material is in silicon carbide and if the substrate is in silicon.

For this purpose, a carrier substrate (target) may be used having a superficial insulator layer and the first substrate may be transferred with the layer of semiconductor material onto the insulator layer of the carrier substrate.

It also possible, in alternate or supplemental manner, to form an insulator layer on the layer of semiconductor material before ion implantation step b).

The insulator layer of the carrier substrate and/or the insulator layer formed on the layer of semiconductor material may for example be an oxide layer.

At the end of the process, that is to say after step e), it is possible to increase the thickness of the layer of semiconductor material by homoepitaxy.

In one particular embodiment of the process, for the formation of substrates intended for optoelectronics, a superficial layer in silicon carbide can be made on which a layer of gallium nitride can be formed.

The gallium nitride layer may be formed by heteroepitaxy.

Other characteristics and advantages of the invention will become clearer with the following description which refers to the figures of the appended drawings. This description relates to one particular embodiment of the invention and is given solely for non-restrictive, illustrative purposes.

Short description of the figures

- Figures 1 to 3 are section views of a first substrate during the preparation stages preceding its transfer onto a carrier substrate or target substrate.

- Figures 4 and 5 are section views illustrating the transfer operation of the first substrate onto the carrier substrate.

- Figure 6 is a section view of the carrier substrate obtained after cleavage of the first substrate.

- Figure 7 is a section view of the substrate in figure 6 obtained after surface treatment and on which a superficial layer of semiconductor material has been made thicker.

- Figure 8 is a section view of the substrate in figure 6 after surface treatment and on which a layer of semiconductor material has been grown.

It is to be noted that, for reasons of clarity, the different layers of material of the structures visible in the figures are not shown to scale; the sizes of some parts are strongly exaggerated.

Detailed description of examples of embodiments of the invention

Figure 1 shows a first substrate 10 in silicon, on which a layer of silicon carbide 12 has been formed.

The layer of silicon carbide is, for example, obtained by surface carburizing the silicon of substrate 10 by reaction between a hydrocarbon and the silicon. This reaction takes place at a temperature in the region of 1350°C and enables a layer of silicon carbide (SiC) to be formed of narrow thickness. The

thickness of the layer of silicon carbide is in the order of 5 to 10 nm.

It can be seen that the process described herein may be used with wafers of large diameter which form the first substrate.

Figure 2 shows an optional step of the process during which a silicon oxide layer 14 is deposited on the SiC layer 12. The silicon oxide layer whose thickness is in the order of 500 nm enables subsequent reduction of the effects of differential thermal dilatations between the layer of silicon carbide and a carrier substrate in silicon, described below, onto which this layer is transferred.

The thickness of the oxide layer is not critical and may be chosen from a wide range of values.

Figure 3 shows the formation in the first substrate 10 of a cleavage zone 16. The cleavage zone is formed by ion implantation, with hydrogen ions for example. Implantation dose and energy are chosen in relation to the thickness of the SiC layer 12 and oxide layer 14 so as to form the cleavage zone preferably under the superficial layer 12, in substrate 10, as close as possible to its surface, that is to say as close as possible to the Si/SiC interface.

For a more detailed description of the formation of a cleavage zone, reference may be made to document (2) already cited.

The cleavage zone 16 delimits, in silicon substrate 10, a superficial layer of silicon 18.

As shown in figure 4, the first substrate 10, provided with the layer of silicon carbide 12 and the oxide layer 14, is brought to a second carrier substrate 20, this second substrate is in silicon and

on one of its surfaces it has a layer of silicon oxide 24. The carrier substrate 20 is also called a target substrate.

Substrates 10 and 20 are oriented so that the oxide layers 14 and 24, previously cleaned to permit bonding, face one another.

It is to be noted at this point that the oxide later 24 formed on the surface of the second substrate 20, and the oxide layer 14 of the first substrate 16 are optional.

Figure 5 shows the transfer of the first substrate 10 onto the second substrate 20, by contacting the free surfaces of these substrates, respectively formed by the oxide layers.

The oxide layers are bonded to one another by molecular adhesion. Bonding may be reinforced by appropriate heat treatment.

The heat treatment is continued, or another heat treatment is applied, with a sufficient heat schedule to cause cleavage of the structure in figure 5 along the cleavage zone 16. Cleavage is symbolized by arrows.

After cleavage and after removal of the remaining solid part of the first substrate, the structure shown in figure 6 is obtained. The orientation of the second substrate 20 in figure 6 has undergone a 180° change relative to figure 5.

The structure in figure 6 comprises, in this order, carrier substrate 20, oxide layer 24 formed on its surface, oxide layer 14 derived from the first substrate, silicon carbide layer 12 and the thin layer of superficial silicon 18 also derived from the first substrate.

The superficial layer 18 is then removed from the structure, for example by wet chemical attack using a solution of TMAH.

To fabricate sensors or micromechanical parts with a membrane in silicon carbide, the thickness of the silicon carbide layer 12 can be increased by silicon carbide epitaxy on this layer.

This operation is shown in figure 7 in which the thickness of the SiC layer 12 is increased.

With epitaxy it is possible to increase the thickness of the silicon carbide layer up to values of 500 nm to 1 µm for example.

Structures with suspended SiC membrane can be easily obtained by partial etching of the underlying oxide layers 24, 14.

In another application of the substrate, for example in the area of optoelectronics, a semiconductor material may be formed by heteroepitaxy on SiC layer 12 after removing the superficial layer of silicon.

Figure 8 shows such application in which a layer of GaN 30 is formed on the uncovered silicone carbide layer 12.

The preceding description only forms a particular example of embodiment of the invention. The materials chosen and the thickness of the layers may vary over a large range in relation to intended applications.

The process of the invention may be applied to materials other than SiC, such as for example AsGa, GaN or ferroelectric material.

It then also allows layers of material of good quality to be obtained, that are little sensitive to thermal dilatations and whose thickness may be adjusted at the end of the process, by epitaxy for example.

Also, the materials used for the first and second substrates may be other than silicon. Sapphire for example may be used.

CITED DOCUMENTS

(1) *"Smart Cut" Process offers SiC structures on Silicon Wafers*, Brian Dance, 58/Semiconductor International, May 1997

(2) EP-A-0 533 551

CLAIMS

1. Process for fabricating a structure comprising a carrier substrate (20) and a layer of semiconductor material (12) on one surface of the carrier substrate, the process comprising the following successive steps:

a) forming a layer of semiconductor material (12) on one surface of a first substrate (10),

b) implanting ions in the first substrate, under said surface, in the vicinity of the layer of semiconductor material, to form a zone (16), called a cleavage zone, which delimits a superficial layer (18) in the first substrate (10), in contact with the layer of semiconductor material (12),

c) transfer of the first substrate (10), with the layer of semiconductor material (12), onto the carrier substrate (20), the layer of semiconductor material (12) being made integral with the carrier substrate (20),

d) providing energy to cause cleavage of the first substrate along the cleavage zone (16), the superficial layer (18) of the first substrate remaining integral with the layer of semiconductor material (12) and with the carrier substrate (20) during this cleavage,

e) removing said superficial layer (18) to uncover the layer of semiconductor material (12).

2. Process according to claim 1, in which, during step d) the supply of energy is made in a form chosen from among a supply of thermal energy, a supply of mechanical energy, or a supply of a combination of these energies.

3. Process according to claim 1, in which step e) is implemented according to a removal mode chosen from among wet or dry chemical etching, polishing, oxidation followed by etching, or a combination of these modes.

4. Process according to claim 1, in which the first substrate (10) is a silicon substrate and the layer of semiconductor material (12) is a layer of silicon carbide.

5. Process according to claim 4, in which the layer of semiconductor material (12) in silicon carbide is obtained by causing the silicon of the first substrate (10) to react with a hydrocarbon.

6. Process according to claim 1, in which an insulator layer (14) is formed on the layer of semiconductor material (12) before ion implantation step b).

7. Process according to claim 1, in which a carrier substrate (20) is used which has a superficial insulator layer (24) and in which, during step c), the first substrate (10) is transferred with the layer of semiconductor material (12) onto the insulator layer (24) of the carrier substrate.

8. Process according to claim 2 or 3, in which the insulator is an oxide.

9. Process according to claim 1, in which, after step e), on the layer of semiconductor material (12),

epitaxial growth of the same material is made in order to increase the thickness of the layer of semiconductor material (12).

10. Process according to claim 4, in which, after step e), on silicon carbide layer (12), a layer (30) of GaN is formed.

11. Process according to claim 1, in which the layer of semiconductor material (12) is made integral with the carrier substrate (20) by heat treatment.

12. Process according to claim 11 in which said heat treatment, to render the layer of semiconductor material integral with the carrier substrate, is extended to additionally cause the cleavage of step d).

B 12946.3 EW

Declaration, Power Of Attorney and Petition

WE (I) the undersigned inventor(s), hereby declare(s) that :

My residence, post office address and citizenship are as stated below next to my name,

We (I) believe that we are (I am) the original, first, and joint (sole) inventor(s) of the subject matter which is claimed and for which a patent is sought on the invention entitled

"PROCESS FOR FABRICATING A STRUCTURE OF SEMICONDUCTOR-ON-INSULATOR TYPE, IN PARTICULAR SiCOI"

the specification of which

☐ is attached hereto.

☐ was filed on

as Application Serial No.

and amended on

☒ was filed as PCT international application

Number PCT/FR99/00155

on January 27, 1999

and was amended under PCT Article 19

on

We (I) hereby state that we (I) have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

We (I) acknowledge the duty to disclose information known to be material to the patentability of this application as defined in Section 1.56 of Title 37 Code of Federal Regulations.

We (I) hereby claim foreign priority benefits under 35 U.S.C. § 119 (a)-(d) or § 365 (b) of any foreign application(s) for patent or inventor's certificate, or § 365 (a) of any PCT International application which designated at least one country other than the United States, listed below and have also identified below, by checking the box, any foreign application for patent or inventor's certificate, or PCT International application having a filing date before that of the application on which priority is claimed. Prior Foreign Application (s)

Application No.	Country	Day/month/Year	Priority Claimed
98 00899	FRANCE	28 JANUARY 1998	☒ YES ☐ NO
			☐ YES ☐ NO
			☐ YES ☐ NO
			☐ YES ☐ NO

We (I) hereby claim the benefit under Title 35, United States Code, § 119 (e) of any United States provisional application(s) listed below.

(Application Number)	(Filing Date)
(Application Number)	(Filing Date)

We (I) hereby claim the benefit under 35 U.S.C. §120 of any United States application(s), or § 365(c) of any PCT International application designating the United States, listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States or PCT International application in the manner provided by the first paragraph of 35 U.S.C. § 112, I acknowledge the duty to disclose information which is material to patentability as defined in 37 CFR § 1.56 which became available between the filing date of prior application and the national or PCT International filing date of this application.

Application Serial No.	Filing Date	Status (pending, patented, abandoned)

And we (I) hereby appoint : Norman F. Oblon, Registration Number 24,618; Marvin J. Spivak, Registration Number 24,913; C, Irvin McClelland, Registration Number 21,214; Gregory J. Maier, Registration Number 25,599; Arthur I. Neustadt, Registration Number 24,854; Richard D. Kelly, Registration Number 27,757; James D. Hamilton, Registration Number 28,421; Eckhard H. Kuesters, Registration Number 28,870; Robert T. Pous, Registration Number 29,099; Charles L. Gholz, Registration Number 26,395; Vincent J. Sunderdick, Registration Number 29,004; William E. Beaumont, Registration Number 30,996; Steven B. Kelber, Registration Number 30,073; Robert F. Gnuse, Registration Number 27,295; Jean-Paul Lavalleye, Registration Number 31,451; William B. Walker, Registration Number 22,498; Timothy R. Schwartz, Registration Number 32,171; Stephen G. Baxter, Registration Number 32,884; Martin M.,. Zoltick, Registration Number 35,745; Robert W. Hahl, Registration Number 33,893; and Richard L. Treanor, Registration Number 36,379; our (my) attorneys, with full powers of substitution and revocation, to prosecute this application and to transact all business in the Patent Office connected therewith; and we (I) hereby request that all correspondence regarding this application be sent to the firm of OBLON, SPIVAK, McCLELLAND, MAIER & NEUSTADT, P.C., whose post Office Address is : Fourth Floor, 1755 Jefferson Davis Highway, Arlington, Virginia 22202.

We (I) declare that all statements made herein of our (my) own knowledge are true and that all statements made on information and belief are believed to be true ; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such wilful false statements may jeopardise the validity of the application or any patent issuing thereon.

DI CIOCCIO Léa

NAME OF FIRST SOLE INVENTOR

Signature of Inventor

03 juillet 2000

Date

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